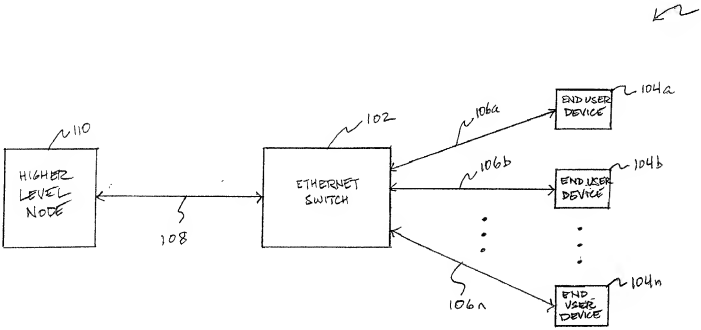

FIG. 1

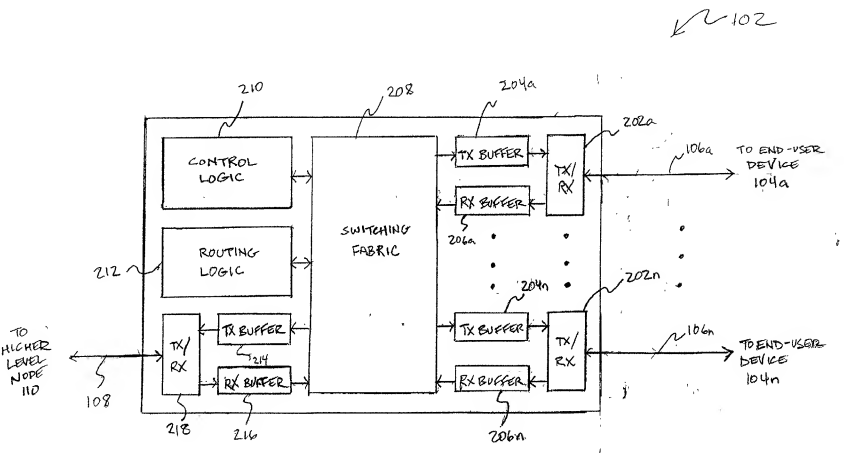
102
210
208
204a
202a
CONTROL LOGIC
ROUTING LOGIC
212
SWITCHING FABRIC
TX BUFFER
RX BUFFER
206a
TX/ RX
106a
TO END-USER DEVICE 104a
204n
202n
206n
106n
TO END-USER DEVICE 104n
TO HIGHER LEVEL NODE 110
108
214
216
218

FIG. 2

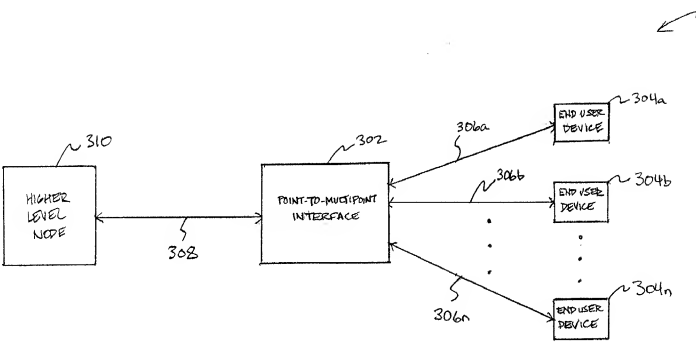

FIG. 3

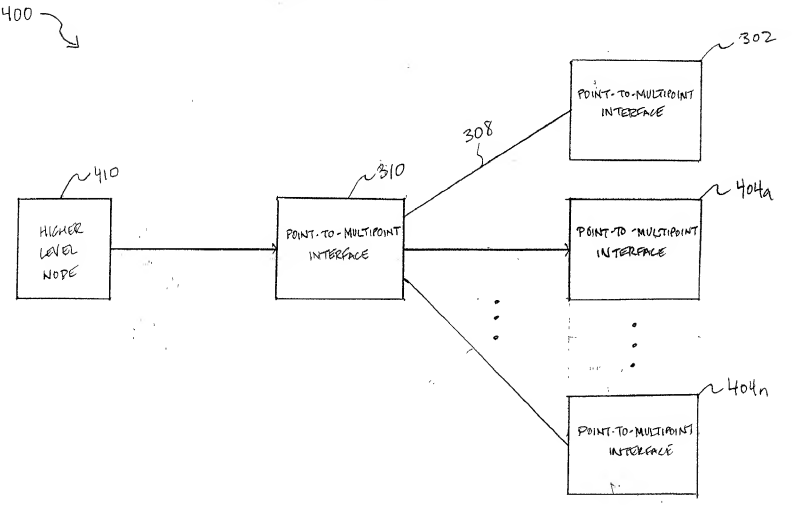
400
302
POINT-TO-MULTIPOINT INTERFACE
308
410
310
HIGHER LEVEL NODE
POINT-TO-MULTIPOINT INTERFACE
404a
POINT-TO-MULTIPOINT INTERFACE
404n
POINT-TO-MULTIPOINT INTERFACE

FIG. 4

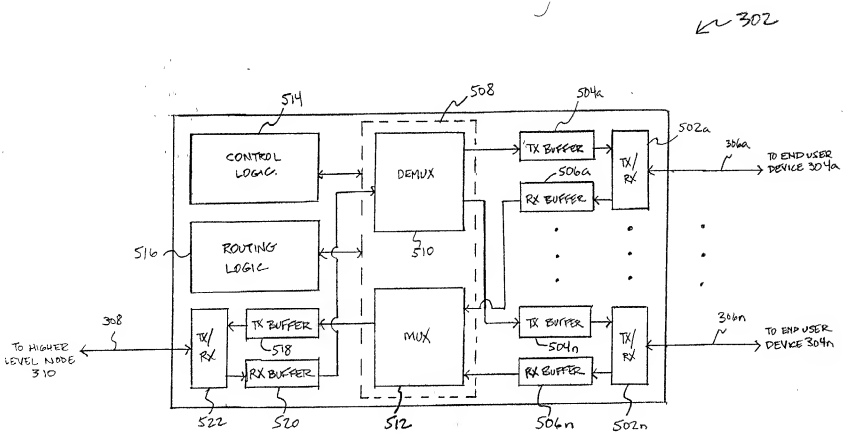
302
514
508
504a
CONTROL LOGIC
DEMUX
TX BUFFER
502a
306a
TO END USER DEVICE 304a
506a
RX BUFFER
TX/ RX
516
ROUTING LOGIC
510
308
TO HIGHER LEVEL NODE 310
TX/ RX
TX BUFFER
518
RX BUFFER
MUX
TX BUFFER
504n
RX BUFFER
TX/ RX
306n
TO END USER DEVICE 304n
522
520
512
506n
502n

FIG. 5

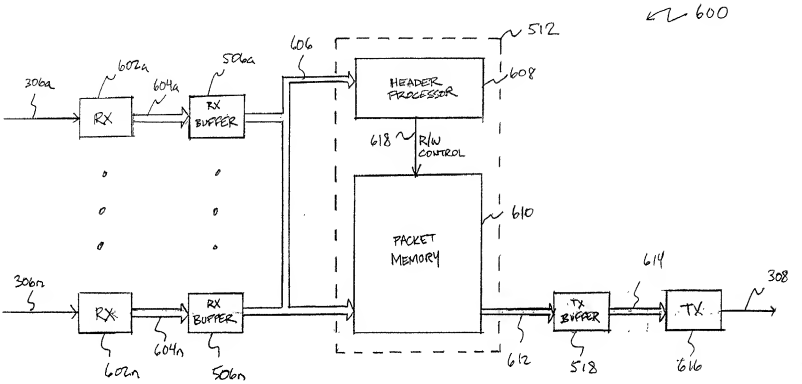
600
512
606
306a
602a
604a
506a
RX
RX BUFFER
HEADER PROCESSOR
608
618
R/W CONTROL
610
PACKET MEMORY
614
306n
602n
604n
506n
612
TX BUFFER
518
TX
616
308

FIG. 6

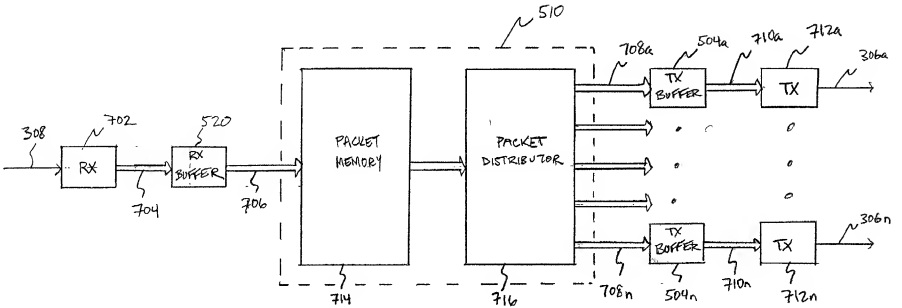
510
708a
504a
710a
712a
306a
308
702
520
RX
RX BUFFER
704
706
PACKET MEMORY
PACKET DISTRIBUTOR
TX BUFFER
TX
306n
714
716
708n
504n
710n
712n

FIG. 7

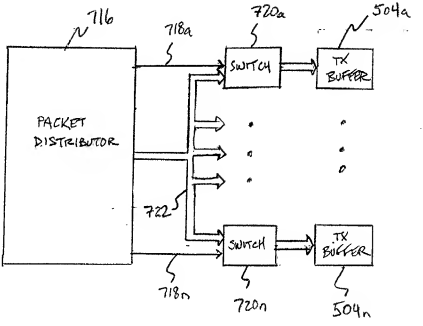
716
718a
720a
504a
PACKET
DISTRIBUTOR
SWITCH
TX
BUFFER
722
SWITCH
TX
BUFFER
718n
720n
504n

FIG. 8

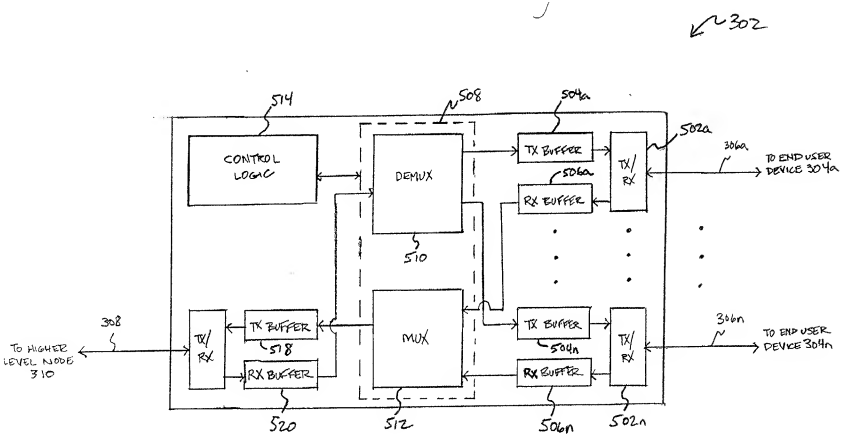
302
514
508
504a
502a
CONTROL LOGIC
DEMUX
TX BUFFER
RX BUFFER
TX/ RX
506a
306a
TO END USER DEVICE 304a
510
308
TO HIGHER LEVEL NODE 310
TX/ RX
TX BUFFER
518
RX BUFFER
520
MUX
512
TX BUFFER
504n
RX BUFFER
506n
TX/ RX
502n
306n
TO END USER DEVICE 304n

FIG. 9

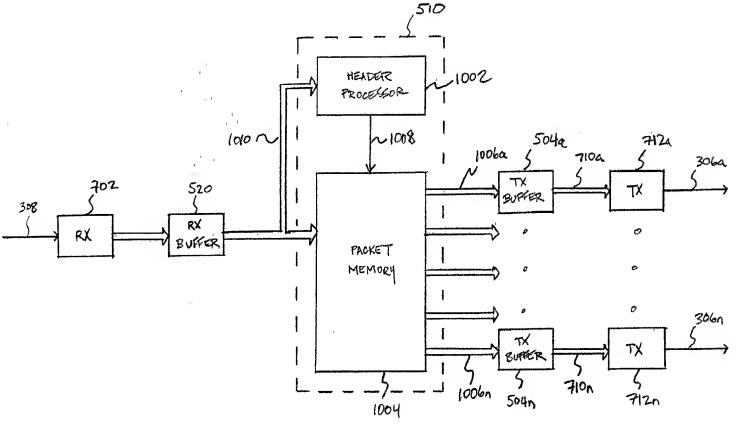
510
HEADER PROCESSOR
1002
1008
1010
1006a
504a
710a
712a
306a
308
702
520
RX
RX BUFFER
PACKET MEMORY
TX BUFFER
TX
306n
1004
1006n
504n
710n
712n

FIG. 10

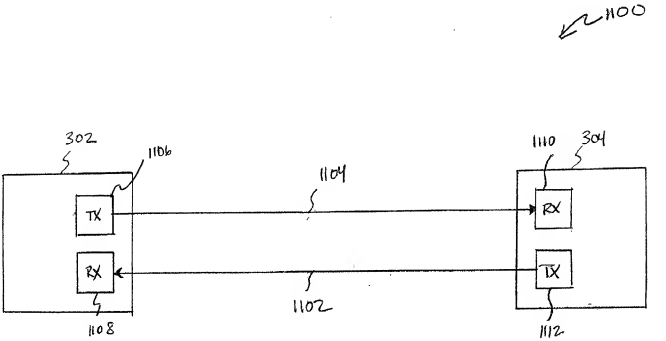

FIG. 11